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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 10/608,530      | 06/30/2003  | Su Ock Chung         | 40296-0004          | 8223             |

26633 7590 03/18/2005

HELLER EHRMAN WHITE & MCAULIFFE LLP  
1717 RHODE ISLAND AVE, NW  
WASHINGTON, DC 20036-3001

EXAMINER

VINH, LAN

| ART UNIT | PAPER NUMBER |
|----------|--------------|
|----------|--------------|

1765

DATE MAILED: 03/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

|                              |                                      |                                      |  |
|------------------------------|--------------------------------------|--------------------------------------|--|
| <b>Office Action Summary</b> | <b>Application No.</b><br>10/608,530 | <b>Applicant(s)</b><br>CHUNG, SU OCK |  |
|                              | <b>Examiner</b><br>Lan Vinh          | <b>Art Unit</b><br>1765              |  |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 30 June 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1 and 2 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 and 2 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 10/605,530.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

*2e*

**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Jeng et al (US 5,792,687)

Jeng discloses method for fabricating a semiconductor device comprising the steps of:

sequentially forming a gate insulating film 3 and a conductive layer 6 for gate electrode on a semiconductor substrate (col 4, lines 18-20)

forming multi-layered hard mask layer comprises of layers 10 (polycide) and 12 (SiN) on the conductive layer, wherein each layer of the multi-layered hard mask layer is formed of materials different from one another (col 4, lines 27-28; fig. 1)

etching to pattern the hard mask layer, the conductive layer 6 and the gate insulting film 3 using a gate electrode mask to form stacked structure of gate insulating film pattern, a gate electrode and a hard mask layer pattern (col 4, lines 40-43; fig. 1)

forming an insulating film spacer 18 on a sidewall of the stacked structure (col 4, lines 58-61)

forming an interlayer insulating film 22 on the entire surface of the structure (col 5, lines 18-20; fig. 3)

etching the interlayer insulating film using a polysilicon layer and the spacers as a mask/landing plug contact etching mask to form a landing plug contact hole 32 exposing the semiconductor substrate (col 5, lines 66-67; fig. 5)

forming conductive layer 41 for a landing plug on the entire surface to fill the landing plug contact hole 32 (col 6, lines 34-36; fig. 6)

planarizing the conductive layer 41 for a landing plug to form a landing plug (col 6, lines 39-41)

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeng et al (US 5,792,687) in view of Kumar et al (US 6,696,365)

Jeng's method has been described above. Unlike the instant claimed invention as per claim 2, Jeng fails to specifically disclose using a hard mask comprises a stacked structure of nitride film/oxide film/nitride film

Kumar, in a process for etching a semiconductor device, discloses using a hard mask stack comprises of nitride film/oxide film/nitride film (col 2, lines 44-46; fig. 4)

Hence, one skilled in the art at the time the invention was made would have found it obvious to modify Jeng's hard mask by using a hard mask stack as per Kumar because Kumar discloses that typical multilayer hard mask stack used for patterning silicon prior to etching deep trenches comprises in sequence a thin layer of oxide, a layer of nitride and a layer of hard mask (col 1, lines 14-17)

### ***Conclusion***

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 1765

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to be 'V. Han' or similar, with a stylized flourish at the end.

LV

March 16, 2005